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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/829,559	04/22/2004	Asher Hazanchuk	ALT.P030 (A1252)	6357

27296 7590 10/28/2010

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EXAMINER	
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ART UNIT	PAPER NUMBER
2193	

MAIL DATE	DELIVERY MODE
10/28/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/829,559	HAZANCHUK ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 August 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3 and 5-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3 and 5-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment filed 08/16/2010.

2. Claims 1, 3 and 5-26 are pending in this application. Claims 1, 11, 17 and 21-22 are independent claims. In Amendment, claims 2 and 4 are cancelled and claims 25-26 are added. This Office Action is made final.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 1, 3, 5-16, 21 and 23-24 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 1, 3, 5-16, 21 and 23-24 cite a method for performing multiplication in accordance with a mathematical algorithm. However, these method claims fail to tie to specific machine or apparatus for realizing the implementation wherein it is unclear as what is the target device in the preamble. Therefore, claims 1, 3, 5-16, 21 and 23-24 are directing to non-statutory subject matter.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 3, 5-7, 9 and 11-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bhandal et al. (U.S. 6,711,602) in view of Schier et al. (U.S. 7,046,723).

Re claim 1, Bhandal et al. disclose in Figures 1-22 a method for performing multiplication of a first number with a second number (e.g. abstract and Figure 8 as general architecture of multiplier), comprising: generating a product by multiplying a first plurality of bits from a first number and a first plurality of bits from a second number (e.g. Figure 11B wherein SRC1_L as B is multiplying with SRC2_L as D by B*D) using a digital signal processor (DSP) where a largest dimension of multiplication supported by the DSP is under that which supports multiplying the first and second numbers (e.g. Figures 11-12 wherein first and second numbers are considered as the source 1 and source 2 respectively and the multiplication is done on the portion of sources as high portion or lower portion of the source by multiplier 800 in Figure 8 wherein the multiplier 800 performs 16 bits multiplication of 32 bits operands); a product of a second plurality of bits from the first number and a second plurality of bits from the second number (e.g. Figure 11B wherein SRC1_H as A is multiplying with SRC2_H as C by A*C) wherein the second plurality of bits from the first number is fewer than the bits of the first number and the second plurality of bits from the second number is fewer than the bits of the second number (e.g. the number of bits of high or low portion of the source is less than the whole bits of source as seen in Figures 11-12 wherein either high or low portion is only 16 bits compare to 32 bits of the source); scaling the product with respect

to a position of the first plurality of bits from the first number and a position of the first plurality of bits from the second number (e.g. by shifter 810 in Figure 8) and scaling the stored value with respect to a position of the second plurality of bits from the first number and a position of the second plurality of bits from the second number (e.g. by shifter 811 in Figure 8); and summing a scaled product and a sealed stored value to generate a value representing a product of the first number and the second number (e.g. output of adder 820 in Figure 8 and Figure 11B), wherein the first number and the second number each have a number of bits equal to or greater than a total of the first and second plurality of bits (e.g. Figure 11B wherein each of input operands consist of 32 bits and each of input multiplied operand is 16 bits).

Bhandal et al. fail to disclose the multiplier is done on a target device and the second product is retrieved from a memory. However, Schier et al. disclose in Figures 1-4 the multiplier is done on a target device (e.g. abstract as can be FPGAs) and the second product is retrieved from a memory (e.g. any intermediate product from the LUT in Figures 1-4 as b1x).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the multiplier is done on a target device and the second product is retrieved from a memory as seen in Schier et al.'s invention into Bhandal et al.'s invention because it would enable to improve system performance (e.g. col. 3 lines 9-11 and col. 4 lines 9-12).

Re claim 3, Bhandal et al. further disclose in Figures 1-22 the DSP block is configured to multiply two numbers of equal bit length (e.g. 16 bits by 16 bits in Figure 11B).

Re claim 5, Bhandal et al. further disclose in Figures 1-22 scaling the product comprises shifting bits in the product relative to a global least significant bit (e.g. Figures 8 and 11B).

Re claim 6, Bhandal et al. further disclose in Figures 1-22 scaling the stored value comprises shifting bits in the product relative to a global least significant bit (e.g. Figures 8 and 11B).

Re claim 7, Bhandal et al. fail to disclose in Figures 1-22 retrieving a second stored value designated as a product era third plurality of bits from the first number and a third plurality of bits from the second number; retrieving a third gored value designated as a product of a fourth plurality of bits from the first number and a fourth plurality of bits from the second number; scaling the second stored value with respect to a position of the third plurality of bits from the first number and a position of the third plurality of bits from the second number and scaling the third stored value with respect to a position of the fourth plurality orbits from the first number and a position of the fourth plurality of bits from the second number, and summing a scaled second stored value and a scaled third stored value. However, Schier et al.'s disclose in Figures 1-4 retrieving a second stored value designated as a product of a third plurality of bits from the first number and a third plurality of bits from the second number (e.g. b2x in Figure 1); retrieving a third gored value designated as a product of a fourth plurality of bits from the first number and

a fourth plurality of bits from the second number (e.g. b3x in Figure 1); scaling the second stored value with respect to a position of the third plurality of bits from the first number and a position of the third plurality of bits from the second number (e.g. bit shift left in Figures 2-4) and scaling the third stored value with respect to a position of the fourth plurality of bits from the first number and a position of the fourth plurality of bits from the second number (e.g. bit shift left in Figures 2-4), and summing a scaled second stored value and a scaled third stored value (e.g. output of adder 3 in Figure 1).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to retrieving a second stored value designated as a product era third plurality of bits from the first number and a third plurality of bits from the second number; retrieving a third gored value designated as a product of a fourth plurality of bits from the first number and a fourth plurality of bits from the second number; scaling the second stored value with respect to a position of the third plurality of bits from the first number and a position of the third plurality of bits from the second number and scaling the third stored value with respect to a position of the fourth plurality orbits from the first number and a position of the fourth plurality of bits from the second number, and summing a scaled second stored value and a scaled third stored value as seen in Schier et al.'s invention into Bhandal et al.'s invention because it would enable to improve system performance (e.g. col. 4 lines 3-21).

Re claim 9, it has similar limitations cited in claim 7. Thus, claim 9 is also rejected under the same rationale as cited in the rejection of rejected claim 7.

Re claim 11, Bhandal et al. disclose in Figures 1-22 a method for implementing a multiplier to perform multiplication of a first number with a second number (e.g. abstract and Figure 8 as general architecture) utilizing a single DSP (e.g. Figure 11B and Figures 11-12 wherein first and second numbers are considered as the source 1 and source 2 respectively and the multiplication is done on the portion of sources as high portion or lower portion of the source by multiplier 800 in Figure 8 wherein the multiplier 800 performs 16 bits multiplication of 32 bits operands), comprising: configuring a digital signal processor (DSP) to perform multiplication on a first plurality of bits from a first number and a first plurality of bits from a second number (e.g. Figure 11B with product B*D) where the first plurality of bits from the first and second numbers are fewer than the bits forming the first and second number (e.g. the number of bits of high or low portion of the source is less than the whole bits of source as seen in Figures 11-12 wherein either high or low portion is only 16 bits compare to 32 bits of the source); products resulting from multiplication of a second plurality of bits from the first number and a second plurality of bits from the second number (e.g. Figure 11B with product A*C) where the second plurality of bits from the first and second numbers are fewer than the bits forming the first and second number (e.g. the number of bits of high or low portion of the source is less than the whole bits of source as seen in Figures 11-12 wherein either high or low portion is only 16 bits compare to 32 bits of the source); routing an output from the DSP to an adder such that the output from the DSP is scaled according to a position of the first plurality of bits from the first number and a position of the first plurality of bits from the second number (e.g. by shifter 810 in Figure 8), routing

an output as second product to the adder (e.g. adder 820 in Figure 8) such that the output is scaled according to a position of the second plurality of bits from the first number and a position of the second plurality of bits from the second number (e.g. by shifter 811 in Figure 8), and outputting a value representing a product of the second number where the first and second number each have more than the first plurality of bits (e.g. output of adder 820 in Figure 8), wherein the DSP is configured to support multiplication of no more than the first plurality of bits (e.g. 16 bits by 16 bits).

Bhandal et al. fail to disclose the multiplier is done on a target device and the second product is stored/retrieved from a memory. However, Schier et al. disclose in Figures 1-4 the multiplier is done on a target device (e.g. abstract as FPGAs) and the second product is stored/retrieved from a memory (e.g. any intermediate product from the LUT in Figures 1-4 as b1x).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the multiplier is done on a target device and the second product is stored/retrieved from a memory as seen in Schier et al.'s invention into Bhandal et al.'s invention because it would enable to improve system performance (e.g. col. 3 lines 9-11 and col. 4 lines 9-12).

Re claim 12, it has similar limitations cited in claim 7. Thus, claim 12 is also rejected under the same rationale as cited in the rejection of rejected claim 7.

Re claim 13, Bhandal et al. further disclose in Figures 1-22 configuring the DSP comprises determining a number of bits that the DSP will multiply (e.g. Figure 11B).

Re claim 14, Bhandal et al. further disclose in Figures 1-22 determining a number of the second plurality of bits from the first number and a number of the second plurality of bits from the second number (e.g. Figure 11B).

Re claim 15, Bhandal et al. further disclose in Figures 1-22 routing the output from the DSP has the effect of shifting the output from the DSP to a more significant bit position (e.g. left shifting 810 in Figure 8).

Re claim 16, Bhandal et al. fail to disclose in Figures 1-22 routing the output from the memory has the effect of shifting the output from the memory to a more significant bit position. However, Schier et al. disclose in Figures 1-4 routing the output from the memory has the effect of shifting the output from the memory to a more significant bit position (e.g. by bit shift left in Figures 2-4).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add routing the output from the memory has the effect of shifting the output from the memory to a more significant bit position as seen in Schier et al.'s invention into Bhandal et al.'s invention because it would enable to improve system performance (e.g. col. 3 lines 9-11 and col. 4 lines 9-12).

Re claim 17, Bhandal et al. disclose in Figures 1-22 a multiplier to perform multiplication of a first number with a second number (e.g. abstract and Figure 8 as general architecture), comprising: a digital signal processor (DSP) (e.g. Figures 11-12 wherein first and second numbers are considered as the source 1 and source 2 respectively and the multiplication is done on the portion of sources as high portion or lower portion of the source by multiplier 800 in Figure 8 wherein the multiplier 800

performs 16 bits multiplication of 32 bits operands), the DSP configured to perform multiplication on a first plurality of bits from a first number and a first plurality of bits from a second number (e.g. Figure 11B to produce B*D); a product resulting from multiplication of a second plurality of bits from the first number and a second plurality of bits from the second number (e.g. Figure 11B to produce A*C) where the second plurality of bits from the first number is less than the bits forming the first number and the second plurality of bits from the second number is less than the bits forming the second number (e.g. the number of bits of high or low portion of the source is less than the whole bits of source as seen in Figures 11-12 wherein either high or low portion is only 16 bits compare to 32 bits of the source); and an adder that sums (e.g. by adder 820 in Figure 8) a scaled output of the DSP and a scaled output of the second product to output a value representing a product of the first and second number where the first and second number each have more than the first plurality of bits (e.g. by shifters 810 and 811 respectively).

Bhandal et al. fail to disclose the second product is stored/retrieved from a memory. However, Schier et al. disclose in Figures 1-4 the second product is stored/retrieved from a memory (e.g. any intermediate product from the LUT in Figures 1-4 as b1x).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the second product is stored/retrieved from a memory as seen in Schier et al.'s invention into Bhandal et al.'s invention because it would enable to improve system performance (e.g. col. 3 lines 9-11 and col. 4 lines 9-12).

Re claim 18, Bhandal et al. fail to disclose in Figures 1-22 the DSP, the memory, and the adder reside on a field programmable gate array. However, Schier et al. disclose in Figures 1-4 the DSP, the memory, and the adder reside on a field programmable gate array (e.g. abstract).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the DSP, the memory, and the adder reside on a field programmable gate array as seen in Schier et al.'s invention into Bhandal et al.'s invention because it would enable to improve system performance (e.g. col. 3 lines 9-11 and col. 4 lines 9-12).

Re claim 19, it has similar limitations cited in claim 7. Thus, claim 19 is also rejected under the same rationale as cited in the rejection of rejected claim 7.

Re claim 20, Bhandal et al. further disclose in Figures 1-22 the adder sums a sealed output of the second memory with the scaled output of the DSP and the scaled output of the memory (e.g. by adder 820 or adder 3).

Re claim 21, Bhandal et al. disclose in Figures 1-22 a method for implementing a multiplier to perform multiplication of a first number with a second number (e.g. abstract and Figure 8 as general architecture), comprising: configuring a digital signal processor (DSP) (e.g. Figures 11-12 wherein first and second numbers are considered as the source 1 and source 2 respectively and the multiplication is done on the portion of sources as high portion or lower portion of the source by multiplier 800 in Figure 8 wherein the multiplier 800 performs 16 bits multiplication of 32 bits operands), to perform multiplication on a first n bits from a first number and a first n bits from a second

number, wherein a largest dimension multiplier supported by the DSP is an nxn multiplier (e.g. by product B*D in Figure 11B); products resulting from multiplication of a second m bits from the first number and a second m bits from the second number (e.g. by product A*C in Figure 11B); routing an output from the DSP to an adder (e.g. adder 820 in Figure 8) such that the output from the DSP is scaled according to a position of the first n bits from the first number and a position of the first n bits from the second number (e.g. by shifter 810 in Figure 8); routing an output of the second product to the adder such that the output from the memory is sealed according to a position of the second m bits from the first number and a position of the second m bits from the second number (e.g. by shifter 811 in Figure 8); and outputting a value representing a product of the first and second number where the first and second number each have at least n + m number of bits (e.g. output of adder 820 in Figure 8 and Figure 11B).

Bhandal et al. fail to disclose the multiplier is on a field programmable gate array and the second product is retrieved from a memory. However, Schier et al. disclose in Figures 1-4 the multiplier is on a field programmable gate array (e.g. abstract) and the second product is retrieved from a memory (e.g. any intermediate product from the LUT in Figures 1-4 as b1x).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the multiplier is on a field programmable gate array and the second product is retrieved from a memory as seen in Schier et al.'s invention into Bhandal et al.'s invention because it would enable to improve system performance (e.g. col. 3 lines 9-11 and col. 4 lines 9-12).

Re claim 22, Bhandal et al. disclose in Figures 1-22 a multiplier to perform multiplication of a first number with a second number (e.g. abstract and Figure 8 as general architecture) comprising: a digital signal processor (DSP) configured to perform n*n multiplication on a first plurality of bits from a first number and a first plurality of bits from a second number (e.g. produce B*D in Figure 11B with 16x16 bits multiplication), wherein a largest dimension of multiplication supported by the DSP is under that which supports multiplying the first and second numbers (e.g. Figures 11); products resulting from multiplication of a second plurality of bits from the first number and a second plurality of bits from the second number (e.g. produce A*C in Figure 11B with 16x16 bits multiplication); and an adder that sums a scaled output of the DSP and a scaled (e.g. scaling by shifters 810 and 811 in Figure 8) output of the memory to output a value representing a product of the first and second number (e.g. by adder 820 in Figure 8) where the first and second number each have more than n bits (e.g. each have 32 bits or 2n total in Figure 11B).

Bhandal et al. fail to disclose the second product is stored/retrieved from a memory. However, Schier et al. disclose in Figures 1-4 the second product is stored/retrieved from a memory (e.g. any intermediate product from the LUT in Figures 1-4 as b1x).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the second product is stored/retrieved from a memory as seen in Schier et al.'s invention into Bhandal et al.'s invention because it would enable to improve system performance (e.g. col. 3 lines 9-11 and col. 4 lines 9-12).

Re claim 23, Bhandal et al. further disclose in Figures 1-22 scaling the product comprising routing the product directly to an adder at inputs of appropriate significance (e.g. by shifter 810 in Figure 8 as an example in Figure 11B by shifting down the upper portion).

Re claim 24, Bhandal et al. further disclose in Figures 1-22 scaling the stored value comprises routing the stored value directly to an adder at inputs of appropriate significance (e.g. by shifter 810 in Figure 8 as an example in Figure 11B by shifting down the upper portion).

Re claim 25, Bhandal et al. further disclose in Figures 1-22 the stored value is retrieved from a location off of the DSP (e.g. memory is not part of DSP).

Re claim 26, Bhandal et al. further disclose in Figures 1-22 the memory is off of the DSP (e.g. memory is not part of the DSP).

Response to Arguments

7. Applicant's arguments filed 08/16/2010 have been fully considered but they are not persuasive.

a. The applicant argues in pages 9-11 for claims rejected under 35 U.S.C. 103(a) that the primary reference by Bhandal fails to disclose the limitations cited the claim 1, particularly the limitations "where a largest dimension...than the bits of the second number".

The examiner respectfully submits that these limitations are clearly and expressively seen in the primary reference by Bhandal as previously rejected and

explained. Generally, the examiner interprets the limitations as using a DSP to generate a first product of a first set of bits from first and second numbers and generate a second product of a second of bits from the first and second numbers wherein both first set of bits and second of bits are fewer than the total bits of the first and second numbers. With this interpretation, any of Figures 11, particularly Figure 11B would anticipate the language of claim 1 wherein the DSP is (can be partial or whole) the processing device in Figures 5 and 8. Specifically the first and second products are the products of A*C and B*D wherein the size each of A, B, C and D is fewer than the first number (as AB) and second number as (CD).

b. The applicant argues in page 12 first paragraph for claims that the Office acknowledge Bhandal does not disclose "retrieving a stored value ….fewer than the bits of the second number" (see 04/14/2010 OA p.5) and replied on Schier, however the secondary reference by Schier fails to disclose the breakdown or partial multiplication instead of complete or entire multiplication of two numbers.

The examiner respectfully submits that the previous Office action did not completely acknowledge the above alleged limitations, but rather only the limitation of retrieve the second product from memory instead of actual or direct multiplication. Generally, the examiner replies on the secondary reference to show/combine the concept of performing direct multiplication can be done/replaced by lookup table to produce the result of multiplying two input numbers.

c. The applicant argues in pages 12-14 for claims that the rejection does not have (1) the basis for combining the references; (2) there is no need or motivation to add a further product from the memory; and (3) the interpretation by the rejection would teach away from the combination since Schier discloses more advantage by using LUTs so then be no motivation for using any partial results from the DSP disclosed in Bhandal.

The examiner respectfully submits that the applicant has miss-understood the combining of the secondary reference into the primary reference wherein the examiner intends to borrow or apply the concept of LUTs to yield the result of multiplication (e.g. as part of the invention), rather then combining the whole invention of Schier into Bhandal. (1) the rejection does clearly state the advantage of having the LUTs instead of actual computation of multiplication since it would improve the system performance by speed; (2) with the above interpretation, there is no need to add a further product from the memory. This limitation can be seen directly in the primary reference by Bhandal in Figures 11; (3) again, the combination of references would not teach away from the claimed invention since nothing in either reference would indicate the un-combinable of references and further the combination would increase in term of speed of the system.

d. The applicant argues in pages 15-17 for claims that Bhandal and Schier do not teach or suggest the limitations of scaling the product comprising routing the product directly to an adder at inputs of appropriate significance.

The examiner respectfully submits that the rejection does clearly explain how this limitation is anticipated by the primary reference Bhandal. The optional scaling in Figures 11 is the one shifting up/down appropriately before sending to the input of final adder for summing the products at appropriated/desired size/bandwidth of result.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHAT C. DO whose telephone number is (571)272-3721. The examiner can normally be reached on Tue-Fri 9:00AM to 7:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lewis Bullock can be reached on (571) 272-3759. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Chat C. Do/
Primary Examiner, Art Unit 2193

September 20, 2010